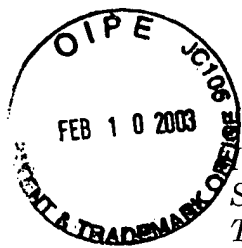


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Koumcan
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PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231 on January 30, 2003.

Christine Sherwood
Signature

Applicant : Janardhanan S. Ajit
Application No. : 10/043,763
Filed : January 9, 2002
Title : SUB-MICRON HIGH INPUT VOLTAGE
TOLERANT INPUT OUTPUT (I/O)
CIRCUIT WHICH ACCOMMODATES
LARGE POWER SUPPLY VARIATIONS

Grp./Div. : 2816
Examiner : Terry D. Cunningham

Docket No. : 41980/PAN/B600

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AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Post Office Box 7068
Pasadena, CA 91109-7068
January 30, 2003

Commissioner:

In response to the Office action of November 29, 2002, please amend the above-identified application as follows:

In the Claims:

Please cancel claims 7-22 and amend claims 1, 3-5 to read as follows. Claims 2 and 6 remain unchanged but are included hereinbelow for the Examiner's convenience.

Sub C1 1. (Amended) A method of protecting an integrated circuit from over voltage, the method comprising: